

# Ultra High Speed Heterojunction Bipolar Transistor Technology

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## Abstract

Scaling of HBTs for high circuit bandwidth and high current gain ( $f_r$ ) and power gain ( $f_{max}$ ) cutoff frequencies is summarized. Key bandwidth limits include scaling of the collector-base junction, the emitter Ohmic contact resistivity, and greatly increased current density. Substrate transfer processes allow submicron collector scaling, and have produced HBTs with 20 dB power gain at 100 GHz. 295 GHz  $f_r$  has been obtained. Key to continued progress is improvement of emitter contacts and reliable operation at  $\sim 10^6$  A/cm<sup>2</sup> current density.

## Introduction

High speed heterojunction bipolar transistors (HBTs) find important applications in complex high frequency ICs. In the commercial arena, ICs for multi-gigabit optical fiber transmission are of major current interest. In military applications, fast HBTs are required for analog-digital and digital-analog converters (ADCs and DACs), and direct digital frequency synthesizers (DDFSs) used in microwave radar and communications. Greatly increased instantaneous bandwidth is sought for future military radar systems now in development; this demands large increases in both the bandwidth and dynamic range of the mixed-signal ICs employed.

In ADCs and DACs, very high resolution is obtained by using oversampling techniques, with clock frequencies  $\approx 100 \times$  the signal bandwidths involved. Further, to avoid ADC metastability errors when comparator inputs are near switching thresholds, circuit time constants must be much smaller the periods of the clock signals employed. Similar constraints apply to high-resolution DACs. High-resolution DACs and ADCs consequently require transistor bandwidths  $10^2:1$  to  $10^4:1$  larger than the signal frequencies involved. Transistors with several hundred GHz  $f_r$  and  $f_{max}$  would enable high-resolution microwave mixed-signal ICs.

In addressing these applications, III-V bipolar transistors must compete with their Silicon counterparts. III-V HBTs offer strong heterojunctions, hence very high base doping for low base resistance, and high electron velocities in the collector, leading to small transit times. Against these

advantages, III-V HBTs have been much less aggressively scaled than Si/SiGe HBTs in either lithographic dimensions or current density. For best transistor performance, we must combine the superior material transport properties of the III-V semiconductors with submicron scaling.

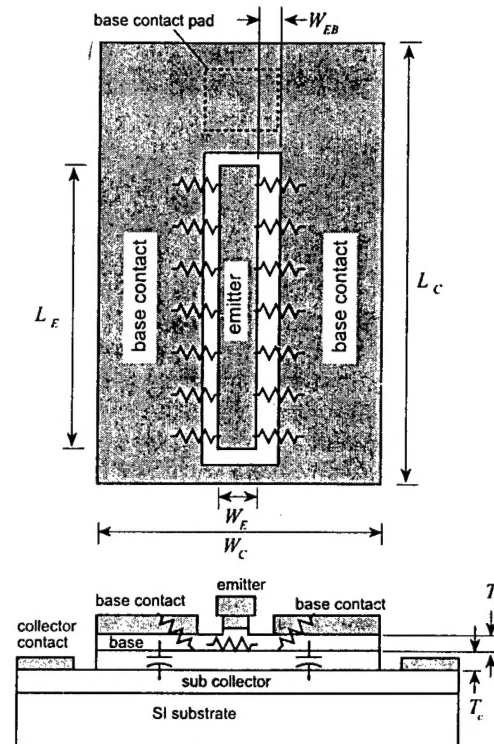


Figure 1: Standard mesa HBT

## HBT Scaling

Transistor bandwidths can be increased by scaling, decreasing the device's lithographic and epitaxial dimensions (Figure 1). For a  $\gamma:1$  improvement in all device transit times and RC delays, hence a  $\gamma:1$  improvement in  $f_r$ ,  $f_{max}$ , and a  $\gamma:1$  speed improvement in an arbitrary circuit using the device, device parameters must scale [1] as in Figure 2. Each 2:1 increase in transistor bandwidth requires a 2:1 thinner collector layer, and 4:1 narrower emitter-base and collector-base junctions. Additionally, the emitter contact resistance per unit area,  $\rho_e$ , must also be improved 4:1, and the current density increased 4:1.

parameter	symbol	scaling law
collector epitaxial thickness	$T_c$	$\gamma^{-1}$
base epitaxial thickness	$T_b$	$\gamma^{-1/2}$
emitter stripe width	$W_e$	$\gamma^{-2}$
collector-base junction width	$W_c$	$\gamma^{-2}$
emitter parasitic resistivity	$\rho_e$	$\gamma^{-2}$
emitter current density	$J_e$	$\gamma^2$
base ohmic contact width	$W_b$	$\gamma^{-2}$
base ohmic contact resistivity	$\rho_{c,b}$	$\gamma^{-2}$

**Figure 2:** Scaling laws for standard mesa HBTs. Base Ohmic contact width and base contact resistivity need *not* be scaled in transferred-substrate HBTs.

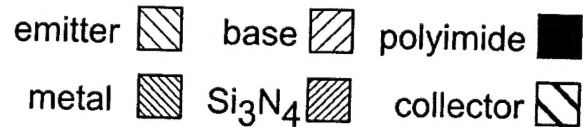
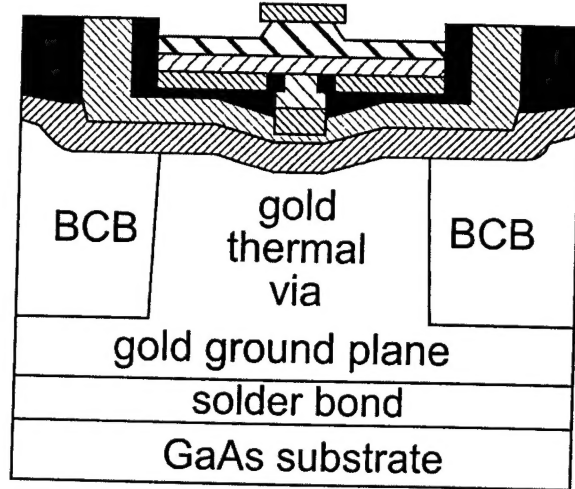
Insofar as these scaling laws can be followed, HBT bandwidth can be arbitrarily increased. Base and collector layer thicknesses in modern HBTs are much larger than the minimum feasible by MBE, hence these can be readily reduced; while breakdown voltage does decrease, this can be addressed by using InP for the collector.

More serious limits include the requirements for narrow junctions, reduced contact resistivity, and increased current density. Emitter contact resistivity must improve rapidly with increases in HBT bandwidth. Emitter current density must increase in proportion to the square of circuit bandwidth. Note that while fast III-V HBT ICs operate at  $\sim 10^5$  A/cm<sup>2</sup> current density, research-grade Si/SiGe HBTs operate at  $10^6$  A/cm<sup>2</sup>. To attain such high current densities in III-V HBTs, heatsinking and reliability must be addressed.

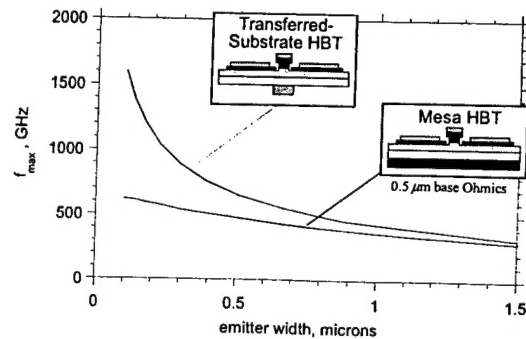
A particularly serious limit to HBT scaling is the required rapid reduction of emitter-base and collector-base junction widths. Emitter widths can be readily scaled using deep submicron projection lithography and precision dry-etch processes for junction definition. In the mesa HBT, the collector-base lies under both the emitter and both base Ohmic contacts. Narrowing the collector junction requires narrowing the base Ohmic contacts; unless the base Ohmic contact resistivity is rapidly improved, this will increase the base resistance. Consequently, the base Ohmic contact resistivity must be improved

rapidly (scaling as  $\gamma^{-2}$ ) as the device is scaled. Alternatively, if the base Ohmic contacts cannot be improved, then the base Ohmic contact width must be kept large, at least one contact transfer length. This then sets a lower limit on the collector-base junction width, and prevents further device scaling.

### Schottky collector contact



**Figure 3:** Transferred-substrate HBT.



**Figure 4:** Fmax, from finite-element analysis, of InAlAs/InGaAs transferred-substrate and mesa HBTs. A 0.5 μm base contact transfer length is assumed.

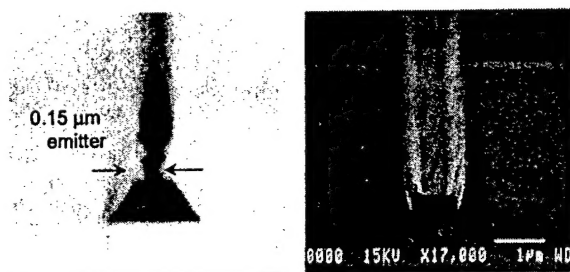
### Transferred-Substrate HBTs

Improvements in base Ohmic contact quality are necessary only because in the mesa HBT the base contacts share common dimensions with the collector junction. In a transferred-substrate HBT

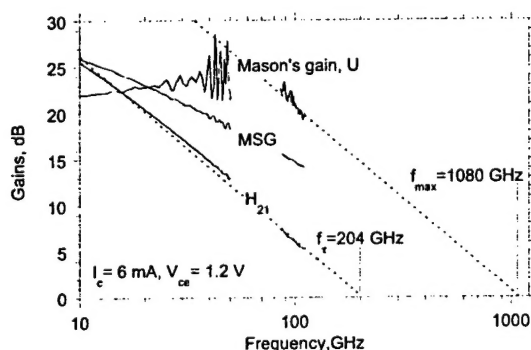
(Figure 3) 2-sided processing of the transistor epitaxial layers [2] results in a transistor with narrow emitter and collector junctions aligned on opposing sides of the base epitaxial layer. The collector and emitter stripe widths can be scaled to deep submicron dimensions, while maintaining wide base Ohmic contacts. Very wide bandwidth devices can be obtained without dramatic improvements in base Ohmic contact quality.

### Results

Transferred-substrate HBTs have been fabricated using a 0.5  $\mu\text{m}$  projection lithography system and using electron-beam lithography (Figure 5)



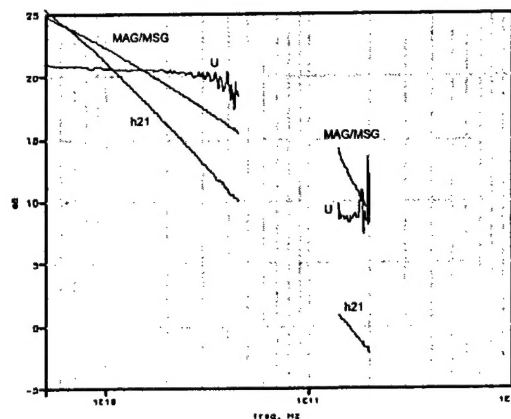
**Figure 5:** E-beam transferred-substrate HBT: test structure with 0.15  $\mu\text{m}$  emitter-base junction (left) and 0.4  $\mu\text{m}$  Schottky collector stripe (right)



**Figure 6:** Gains of a 0.4  $\mu\text{m}$  x 6  $\mu\text{m}$  emitter and 0.7  $\mu\text{m}$  x 10  $\mu\text{m}$  collector HBT. The device exhibits an extrapolated 1 THz  $f_{\text{max}}$ .

Figure 6 shows microwave gains for a deep submicron device fabricated by electron-beam lithography, fabricated by Lee et al [3]. At 100 GHz, the device exhibits 21 dB unilateral power gain, and 15 dB common-emitter maximum stable gain ( $k$  is less than unity). If extrapolated at -20 dB/decade, a 1080 GHz  $f_{\text{max}}$  is determined. We note however that such a 10:1 extrapolation must be treated with considerable caution. More recently-

fabricated devices have been characterized in the 140-220 GHz band [4]. We are still developing methods for precision calibration at these frequencies; Figure 7 shows preliminary data, with ~10 dB unilateral and maximum stable (again,  $k < 1$ ) at 200 GHz. Note that even the DC-45 GHz data indicates that the device of Figure 7 has lower power gain than the device of Figure 6.



**Figure 7:** HBT current gain ( $H_{21}$ ), maximum stable power gain (MSG) and unilateral power gain (U), measured in the DC-45 GHz and 140-200 GHz bands.

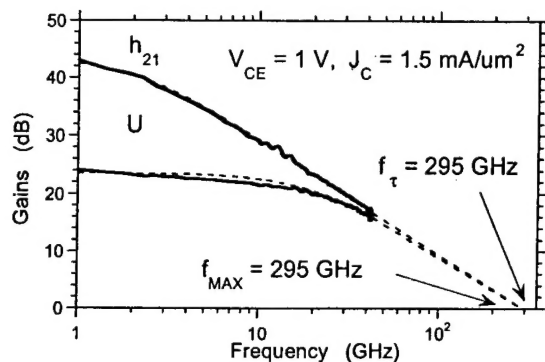
The above devices have very high  $f_{\text{max}}$  but low  $f_T$ . As such they will produce high gains in tuned mm-wave circuits [4], but have a  $f_T/f_{\text{max}}$  ratio too low for effective use in digital and broadband analog ICs. Figure 8 shows RF gains for a device with wider emitter and collector junctions but thinner base and collector epitaxial layers.

Circuit results include 66 GHz master-slave flip-flops [5], DC-80 GHz amplifiers [6], 18-GHz-clock-rate  $\Delta - \Sigma$  ADCs [7], and 185 GHz amplifiers [4].

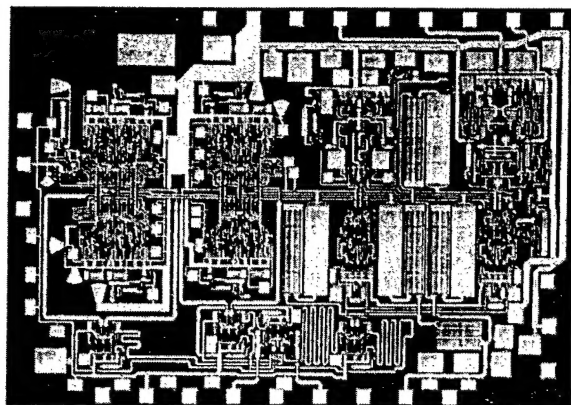
### Limits and Future Challenges

The substrate transfer process greatly facilitates scaling of the HBT collector-base junction, and has produced devices with very low collector-base junction parasitics. These devices consequently have very high  $f_{\text{max}}$ , which can be exploited in very high frequency tuned amplifiers. The low  $R_{bb}$  and  $C_{cb}$  also significantly benefit logic speed, although other circuit time constants are also significant. In the transferred-substrate HBT, as with the mesa HBT, additional scaling limits include required high current density (this is of particular importance in digital ICs [1]) and low emitter contact resistivity. Presently, in our efforts to produce a faster HBT for

digital and mixed-signal circuits, improving upon the HBT of Figure 8, the major challenge has been reduction of the emitter contact resistivity; efforts to increase  $f_T$  through use of thinner collectors have to date been frustrated by increases in the time constant  $R_{ex}C_{cb}$ . A radical solution would be use of zero-barrier (Schottky) emitter contacts; a more pragmatic one would be InAs contact layers and greatly increased doping.



**Figure 8:** Measured RF gains for an HBT with a 300 Å base and a 2000 Å collector. The emitter and collector stripe widths are 1.0 and 1.5 μm, respectively.



**Figure 9:**  $\Delta - \Sigma$  ADC. The IC contains approximately 150 HBTs and operates at 18 GHz clock rate.

It should also be emphasized that high  $f_{max}$  can be obtained without substrate transfer, given extremely low base contact resistivity. Recent results by Dvorak et al [8] using low-resistivity contacts to a GaAsSb base are the best example of this approach. Highest HBT performance will be obtained by combining substrate transfer with the lowest-available base contact resistivity.

## Acknowledgements

This work was supported by the ONR under grants N0014-99-1-0041, N00014-01-1-0065, N00014-01-1-0066, N00014-01-1-0024, N00014-98-1-0750, and N00014-98-1-0830 (D. Purdy, D. VanVechten, M. Yoder, J. Zolper), by the AFOSR under grant F4962096-1-0019 (H. Schlossberg), and by the ARO under the Quasi-Optical MURI PC249806 (J. Harvey).

## References

- [1] M. Rodwell et. al., "Scaling of InGaAs/InAlAs HBTs for High Speed Mixed-Signal and mm-Wave ICs", International Journal of High Speed Electronics and Systems, *to be published*
- [2] Q. Lee, et. al., "Submicron transferred-substrate heterojunction bipolar transistors", IEEE Electron Device Letters, Vol. 20, No. 8, August 1999, pp. 396-398.
- [3] Q. Lee, et al "Submicron transferred-substrate heterojunction bipolar transistors with greater than 1 THz fmax", postdeadline paper, 1999 IEEE Device Research Conference, June, Santa Barbara, CA.
- [4] M. Urteaga, et al, "185 GHz Monolithic Amplifier in InGaAs/InAlAs Transferred -Substrate HBT Technology", Submitted to the 2001 MTT-S International Microwave Symposium, .
- [5] Q. Lee et al "66 GHz static frequency divider in transferred-substrate HBT technology" 1999 IEEE RF/Microwave monolithic circuits symposium, June, Anaheim, CA.
- [6] S. Krishnan, et al, "Broadband lumped HBT amplifiers." Electronics Letters, pp.466-7, Vol. 36, No.5.
- [7] S. Jaganathan et al "An 18 GHz clock rate continuous-time Delta-Sigma modulator implemented in InP transferred-substrate HBT technology", 2000 IEEE GaAs IC Symposium, November, Seattle, Wa.
- [8] Dvorak and Bolognesi, 2000 International Electron Device Meeting, San Francisco, December.